segments providing communication between cells of the cell architecture.

3. (Amended) The bus system according to claim 7, wherein the unit includes a plurality of CPUs in a multi-dimensional arrangement.

4. (Amended) The bus system according to claim 7, wherein the unit includes a plurality of arithmetic logic units in a multi-dimensional arrangement.

15. (Amended) The bus system according to claim 7, further comprising:

a program loading unit, and

wherein the program loading unit performs at least one of a configuration and a reconfiguration for each one of the plurality of nodes and the respective routing table of each one of the plurality of nodes.

22. (Amended) The method according to claim 28, wherein the module having the multi-dimensional cell architecture includes at least one of a field programmable gate array and a dynamically configurable gate array.

23. (Amended) The method according to claim 28, wherein the module having the multi-dimensional cell architecture includes a module having a two-dimensional programmable cell architecture.

24. (Amended) The method according to claim 28, wherein the plurality of bus segments are permanently connected to a continuous bus system without delays.

25. (Amended) The method according to claim 28, wherein the plurality of bus segments are switched by a plurality of registers, each one of the plurality of registers having a time delay and an arbitration.

27. (Amended) The method according to claim 28, wherein the plurality of bus segments are at least one of permanently connected to a continuous bus system without delays and switched by a plurality of registers, each one of the plurality of registers having a time delay and an arbitration.

29. (Amended) The method according to claim 28, the method further comprising the steps of:

entering at least one of a unique determinable relative address and a unique absolute address of a target; and

setting up the plurality of bus segments as a function of the unique determinable relative address and the unique absolute address.

34. (Amended) The method according to claim 28, the method further comprising the step of:

setting up the plurality of bus segments as a function of at least one of a plurality of lookup tables and an at least one of a unique determinable relative address and a unique absolute address of a target.

35. (Amended) The method according to claim 28, the method further comprising the step of:

setting up the plurality of bus segments via a plurality of requests to a plurality of nodes,

wherein a set of requests to a single node of the plurality of nodes are arbitrated if the set of requests includes more than one request.

36. (Amended) The method according to claim 28, the method further comprising the step of:

setting up the plurality of bus segments via a plurality of requests to a plurality of nodes,

wherein a set of requests to a single node of the plurality of nodes are simultaneously processed by the single node.